WHAT IS CLAIMED IS:

1. An apparatus including a decoder for providing a plurality of digital contrast control signals for a video signal, comprising:

a halftone control terminal to convey a halftone control signal with first and second signal statuses corresponding to first and second contrast ranges, respectively, for a video signal;

a plurality of contrast control terminals to convey a plurality of contrast control signals including a first portion corresponding to said first video signal contrast range and including, in successive adjacency, a first least significant bit (LSB) signal, at least one first intermediate significance bit (ISB) signal and a first most significant bit (MSB) signal;

signal decoding circuitry, coupled to said halftone control terminal and said plurality of contrast control terminals, that responds to reception of said halftone control signal and said plurality of contrast control signals by providing a plurality of decoded control signals which, responsive to said first and second halftone control signal statuses, corresponds to said first and second video signal contrast ranges, respectively, wherein said second video signal contrast range is less than said first video signal contrast range; and

buffer circuitry, coupled to said signal decoding circuitry, that responds to reception of said plurality of decoded control signals by providing a like plurality of buffered control signals.

2. The apparatus of claim 1, wherein said signal decoding circuitry comprises signal selection circuitry that responds to said reception of said halftone control signal by selecting one signal within each one of a plurality of pairs of mutually adjacent signals among said first LSB, said at least one first ISB and said first MSB contrast control signals.

3. The apparatus of claim 1, wherein said signal decoding circuitry comprises a plurality of multiplexor circuits each of which is coupled to said halftone control terminal and a respective portion of said plurality of contrast control terminals via which are conveyed mutually adjacent ones of said first LSB, said at least one first ISB and said first MSB contrast control signals.

4. The apparatus of claim 3, wherein said signal decoding circuitry further comprises a logic OR circuit coupled to said halftone control terminal and one of said plurality of contrast control terminals via which said first MSB contrast control signal is conveyed.

5. The apparatus of claim 1, wherein said buffer circuitry comprises a plurality of buffer stages which includes:

a plurality of input inverter circuits each of which responds to reception of a respective one of said plurality of decoded control signals by providing a corresponding inverted control signal; and

a plurality of output inverter circuits, coupled to said plurality of input inverter circuits, each of which responds to reception of said inverted control signal by providing a respective one of said plurality of buffered control signals.

6. The apparatus of claim 5, wherein:

said plurality of output inverter circuits comprises a corresponding plurality of sets of field effect transistors having respective sets of predetermined channel dimensions; and

selected successively adjacent ones of said sets of predetermined channel dimensions vary monotonically.

7. The apparatus of claim 1, wherein:

said plurality of decoded control signals comprises, in successive adjacency, an LSB signal, at least one ISB signal and an MSB signal; and

said MSB decoded control signal, responsive to said first and second halftone control signal statuses, corresponds to said first MSB contrast control signal and said halftone control signal, respectively.

8. The apparatus of claim 1, wherein:

said plurality of contrast control signals further includes a second portion corresponding to said second video signal contrast range and including, in successive adjacency, a second LSB signal, at least one second ISB signal and a second MSB signal; and

said signal decoding circuitry comprises signal selection circuitry that responds to said reception of said halftone control signal by selecting between corresponding ones of said first and second LSB contrast control signals, said first and second ISB contrast control signals, and said first and second MSB contrast control signals.

9. The apparatus of claim 1, wherein:

said plurality of contrast control signals further includes a second portion corresponding to said second video signal contrast range and including, in successive adjacency, a second LSB signal, at least one second ISB signal and a second MSB signal; and

said signal decoding circuitry comprises a plurality of multiplexor circuits each of which is coupled to said halftone control terminal and respective portions of said plurality of contrast control terminals via which are conveyed corresponding ones of said first and second LSB contrast control signals, said first and second ISB contrast control signals, and said first and second MSB contrast control signals.

10. An apparatus including a decoder for providing a plurality of digital contrast control signals for a video signal, comprising:

halftone controller means for conveying a halftone control signal with first and second signal statuses corresponding to first and second contrast ranges, respectively, for a video signal, wherein said second video signal contrast range is less than said first video signal contrast range;

contrast controller means for conveying a plurality of contrast control signals including a first portion corresponding to said first video signal contrast range and including, in successive adjacency, a first least significant bit (LSB) signal, at least one first intermediate significance bit (ISB) signal and a first most significant bit (MSB) signal;

signal decoder means for receiving said halftone control signal and said plurality of contrast control signals and in response thereto generating a plurality of decoded control signals which, responsive to said first and second halftone control signal statuses, corresponds to said first and second video signal contrast ranges, respectively; and

buffer means for receiving said plurality of decoded control signals and in response thereto generating a like plurality of buffered control signals.

11. The apparatus of claim 10, wherein said plurality of contrast control signals further includes a second portion corresponding to said second video signal contrast range and including, in successive adjacency, a second LSB signal, at least one second ISB signal and a second MSB signal.

12. An apparatus including circuitry for controlling and combining video image and on-screen-display (OSD) signals, comprising:

first control circuitry that responds to reception of a first reference signal, a halftone control signal, a plurality of contrast control signals and a clamped video signal by providing a first controlled signal with a contrast-controlled video component, wherein

said halftone control signal includes first and second signal statuses corresponding to first and second contrast ranges, respectively, for said clamped video signal,

said plurality of contrast control signals includes a first portion corresponding to said first video signal contrast range and including, in successive adjacency, a first least significant bit (LSB) signal, at least one first intermediate significance bit (ISB) signal and a first most significant bit (MSB) signal,

said contrast-controlled video component, responsive to said first and second halftone control signal statuses, corresponds to said first and second video signal contrast ranges, respectively, and

said second video signal contrast range is less than said first video signal contrast range;

first signal combining circuitry, coupled to said first control circuitry, that responds to a first combining control signal by receiving and selectively combining an OSD signal and said first controlled signal to provide a first combination signal with said contrast-controlled video component and an OSD component;

second control circuitry, coupled to said first signal combining circuitry, that responds to reception of said first combination signal, said first reference signal and a gain control signal by providing a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component; and

second signal combining circuitry, coupled to said second control circuitry, that responds to a second combining control signal by receiving and selectively combining said second controlled signal and a second reference signal to provide a second combination signal with said contrast-controlled and gain-controlled video component, said gain-controlled OSD component and a reference signal component.

13. The apparatus of claim 12, wherein said first control circuitry comprises:

signal decoding circuitry that responds to reception of said halftone control signal and said plurality of contrast control signals by providing a plurality of decoded control signals which, responsive to said first and second halftone control signal statuses, corresponds to said first and second video signal contrast ranges, respectively;

buffer circuitry, coupled to said signal decoding circuitry, that responds to reception of said plurality of decoded control signals by providing a like plurality of buffered control signals; and

signal magnitude control circuitry, coupled to said buffer circuitry, that responds to reception of said plurality of buffered control signals, said first reference signal and said clamped video signal by providing said first controlled signal.

14. The apparatus of claim 13, wherein said signal decoding circuitry comprises signal selection circuitry that responds to said reception of said halftone control signal by selecting one signal within each one of a plurality of pairs of mutually adjacent signals among said first LSB, said at least one first ISB and said first MSB contrast control signals.

15. The apparatus of claim 13, wherein said signal decoding circuitry comprises a plurality of multiplexor circuits each of which is responsive to reception of said halftone control signal and mutually adjacent ones of said first LSB, said at least one first ISB and first MSB contrast control signals.

16. The apparatus of claim 15, wherein said signal decoding circuitry further comprises a logic OR circuit which is responsive to reception of said halftone control signal and said first MSB contrast control signal.

17. The apparatus of claim 13, wherein said buffer circuitry comprises a plurality of buffer stages which includes:

a plurality of input inverter circuits each of which responds to reception of a respective one of said plurality of decoded control signals by providing a corresponding inverted control signal; and

a plurality of output inverter circuits, coupled to said plurality of input inverter circuits, each of which responds to reception of said inverted control signal by providing a respective one of said plurality of buffered control signals.

18. The apparatus of claim 17, wherein:

said plurality of output inverter circuits comprises a corresponding plurality of sets of field effect transistors having respective sets of predetermined channel dimensions; and

selected successively adjacent ones of said sets of predetermined channel dimensions vary monotonically.

19. The apparatus of claim 13, wherein:

said plurality of decoded control signals comprises, in successive adjacency, an LSB signal, at least one ISB signal and an MSB signal; and

said MSB decoded control signal, responsive to said first and second halftone control signal statuses, corresponds to said first MSB contrast control signal and said halftone control signal, respectively.

20. The apparatus of claim 13, wherein:

said plurality of contrast control signals further includes a second portion corresponding to said second video signal contrast range and including, in successive adjacency, a second LSB signal, at least one second ISB signal and a second MSB signal; and

said signal decoding circuitry comprises signal selection circuitry that responds to said reception of said halftone control signal by selecting between corresponding ones of said first and second LSB contrast control signals, said first and second ISB contrast control signals, and said first and second MSB contrast control signals.

21. The apparatus of claim 13, wherein:

said plurality of contrast control signals further includes a second portion corresponding to said second video signal contrast range and including, in successive adjacency, a second LSB signal, at least one second ISB signal and a second MSB signal; and

said signal decoding circuitry comprises a plurality of multiplexor circuits each of which is responsive to reception of said halftone control signal and corresponding ones of said first and second LSB contrast control signals, said first and second ISB contrast control signals, and said first and second MSB contrast control signals.

22. An apparatus including circuitry for controlling and combining video image and on-screen-display (OSD) signals, comprising:

first controller means for receiving a first reference signal, a halftone control signal, a plurality of contrast control signals and a clamped video signal and in response thereto generating a first controlled signal with a contrast-controlled video component, wherein

said halftone control signal includes first and second signal statuses corresponding to first and second contrast ranges, respectively, for said clamped video signal,

said plurality of contrast control signals includes a first portion corresponding to said first video signal contrast range and including, in successive adjacency, a first least significant bit (LSB) signal, at least one first intermediate significance bit (ISB) signal and a first most significant bit (MSB) signal,

said contrast-controlled video component, responsive to said first and second halftone control signal statuses, corresponds to said first and second video signal contrast ranges, respectively, and

said second video signal contrast range is less than said first video signal contrast range;

first signal combiner means for receiving a first combining control signal and in response thereto receiving and selectively combining an OSD signal and said first controlled signal and generating a first combination signal with said contrast-controlled video component and an OSD component;

second controller means for receiving said first combination signal, said first reference signal and a gain control signal and in response thereto generating a second controlled signal with a contrast-controlled and gain-controlled video component and a gain-controlled OSD component; and

second signal combiner means for receiving a second combining control signal and in response thereto receiving and selectively combining said second controlled signal and a second reference signal and generating a second combination signal with said contrast-controlled and gain-controlled video component, said gain-controlled OSD component and a reference signal component.

23. The apparatus of claim 22, wherein said plurality of contrast control signals further includes a second portion corresponding to said second video signal contrast range and including, in successive adjacency, a second LSB signal, at least one second ISB signal and a second MSB signal.